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# APPLICATION FOR UNITED STATES LETTERS PATENT

# S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Yungpil KIM**, a citizen of Korea, residing at #107-403 Dongyang APT., Songjeong-dong, Icheon-si, Gyeonggi-do, 467-740 KOREA have invented a new and useful **METHOD OF MAKING A MOS TRANSISTOR**, of which the following is a specification.

# METHOD OF MAKING A MOS TRANSISTOR

## TECHNICAL FIELD

**[0001]** The present disclosure relates to semiconductors and, more particularly, to a method of making a metal-oxide-semiconductor (MOS) transistor.

## BACKGROUND

**[0002]** As MOS devices have been integrated at a rapid speed, an existing process using polysilicon as a gate electrode has caused many problems such as high gate resistance, depletion of polysilicon, and boron penetration into a channel area. Such problems have been solved by a process including a metal gate electrode. However, the process of forming a metal gate has caused new problems, such as difficulty in etching a metal and limitations in enduring high-temperature thermal treatment.

**[0003]** Accordingly, a damascene process has been proposed to solve such problems. However, the damascene process uses a chemical mechanical polishing (CMP) process repeatedly, thereby complicating the process, although CMP solved the problems of an existing metal gate process.

**[0004]** To obviate such process complexity, a method of making a MOS transistor using a single CMP process has been proposed. Reference will now be made in detail to a known MOS transistor fabricating method using a single CMP process, examples of which are illustrated in the accompanying drawings. FIGS. 1a through 1c are cross-sectional views illustrating a MOS transistor fabricated according to a known process. Referring to FIG. 1a, a polysilicon gate electrode 5 is formed on a semiconductor substrate 1, and lightly doped drain (LDD) regions 2 are formed on the substrate 1 at both sides of the polysilicon gate electrode 5. Then, a spacer 6 is formed on both lateral walls of the polysilicon gate electrode 5, and source and drain regions 3 are formed on the substrate 1 at both sides of the polysilicon gate electrode 5. Subsequently, a silicide layer 7 is coated on the top of the polysilicon gate electrode 5 and the surface of the source and drain regions 3, and a nitride layer 8 is formed on the entire area of the semiconductor substrate having the source and drain regions 3 and the LDD regions 2 so that the polysilicon gate electrode 5 can be covered. Next, an insulating layer 9 is formed on the nitride layer 8. The nitride layer 8 is usually

between about 300 and about 1000 Å in thickness, and is formed by a plasma enhanced chemical vapor deposition (PECVD) process.

**[0005]** Next, referring to FIG. 1b, the nitride layer 8 and the insulating layer 9 are polished by a CMP process until the top of the polysilicon gate electrode 5 is exposed. The CMP process is performed by over polishing so that the top of the polysilicon gate electrode 5, in uniform thickness, can be exposed completely. Then, a metal layer 10 is deposited, in uniform thickness, on the exposed region of the polysilicon gate electrode 5, the nitride layer 8 and the insulating layer 9. The metal layer 10 is usually less than about 1000 Å and, in some cases, may be between about 500 and about 1000 Å in thickness. The metal layer 10 may be a multilayer of Ti/TiN, Co/TiN, or Co/Ti/TiN.

**[0006]** Referring to FIG. 1c, a thermal treatment is performed on the substrate having the metal layer 10 to transform the polysilicon gate electrode 5 into a metal silicide gate electrode 7. The thermal treatment process may be performed through two steps, i.e., a first step at a temperature of about 400 ℃ to about 600 ℃, and a second step using a rapid thermal process (RTP) at a temperature of about 800 ℃ to about 1000 ℃. Subsequently, the residual metal layer, which has not reacted, is removed.

**[0007]** However, such a method of fabricating a MOS transistor cannot completely transform the polysilicon gate electrode 5 into the metal silicide gate electrode 7 because the area where the metal of the metal layer can be diffused while performing the thermal treatment is insufficient due to the small contact area between the polysilicon gate electrode 5 and the metal layer 10. To obviate such a disadvantage, the thermal treatment process to form the metal silicide gate electrode 7 has to be performed for many hours. However, such a long thermal treatment may cause deterioration of device characteristics because an impurity implanted in source and drain regions 3 may be diffused irregularly.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** FIGS. 1a through 1c are cross-sectional views illustrating a known process of fabricating a MOS transistor.

**[0009]** FIGS. 2a through 2e are cross-sectional views illustrating the disclosed process of fabricating a MOS transistor.

## DETAILED DESCRIPTION

**[0010]** As disclosed herein, a polysilicon gate electrode may be completely transformed into a metal silicide gate electrode by performing a thermal treatment process for a short time because the exposed area of the polysilicon gate electrode, which is in contact with the metal layer, is increased prior to performing the silicide process.

**[0011]** Referring to the example of FIG. 2a, a gate oxide 24 and a polysilicon gate electrode 25 are formed on a semiconductor substrate 21. Then, LDD regions 22 are formed on the surface of the substrate at both sides of the polysilicon gate electrode 25. A spacer 26 is formed on both lateral walls of the polysilicon gate electrode 25, and source and drain regions 23 are formed on the surface of the substrate at both sides of the polysilicon gate electrode 25 including the spacer 26. A self-aligned silicide layer 27 is formed on the top of the polysilicon gate electrode 25 and on the surface of the source and drain regions 23.

**[0012]** As shown in the example of FIG. 2b, the entire area of the semiconductor substrate 21 including the polysilicon gate electrode 25 and source and drain regions 23 are coated with an insulating layer 29. The insulating layer 29 may be formed by using the same material as the spacer 26.

**[0013]** Referring to FIG. 2c, the insulating layer 29 is polished by, for example, a CMP process until the top of the polysilicon gate electrode 25 is exposed. Then, some part of the insulating layer 29 and the spacer 26 are etched by the method of dry-etching and/or wet-etching until the polysilicon gate electrode 25 is exposed to more than about 2/3 of its height. In one particular example, the polysilicon gate electrode 25 is exposed from about 4/6 to about 5/6 of its height. Accordingly, as explained below, as the exposed area of the polysilicon gate electrode 25 is increased, the contact area between the polysilicon gate electrode 25 and a metal layer 30 is expanded, and the polysilicon gate electrode 25 can be completely transformed into a metal silicide gate electrode 31.

**[0014]** Next, referring to FIG. 2d, the entire area of semiconductor substrate shown in FIG. 2c is coated with a metal layer 30 of uniform thickness. In one example, the metal layer 30 is less than 1000 Å thick and may be, for example, between about 500 and about 1000 Å in thickness. The metal layer 30 may be a multilayer comprising transition metals and their alloys such as, for example, Ti/TiN, Co/TiN, or Co/Ti/TiN.

**[0015]** Finally, referring to FIG. 2e, a thermal treatment process is performed on the substrate coated with the metal layer 30 to transform completely the polysilicon gate electrode 25 into a metal silicide gate electrode 31. The thermal treatment may be a rapid thermal process and may be performed through two steps, i.e., a first step at a temperature of about 400℃ to about 600℃, and a second step using RTP at a temperature of about 800℃ to about 1000℃.

**[0016]** As described previously, the contact area between the metal layer and the polysilicon gate electrode is increased because the exposed area of the polysilicon gate electrode is extended or expanded prior to the formation of the metal layer. Therefore, the polysilicon gate electrode reacts actively with the metal layer, and can be completely transformed into the metal silicide electrode. Subsequently, the residual metal layer that has not reacted is removed to complete a disclosed MOS transistor. Accordingly, the disclosed techniques can completely transform the polysilicon gate electrode into the metal silicide electrode through a brief thermal treatment process by extending the contact area between the polysilicide gate electrode and the metal layer prior to the formation of the metal silicide.

**[0017]** The disclosed techniques may be used to produce MOS transistors, each having a gate oxide, a spacer and a gate electrode the top and some part of lateral walls of which are exposed. In addition, the MOS transistor further includes a metal layer that is made of transition metals and their alloys. The disclosed MOS transistors each have a gate electrode that is fully silicided.

**[0018]** Although certain apparatus constructed in accordance with the teachings of the invention have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.